WHAT IS CLAIMED IS:

1. A system for maintaining cache coherency in a CMP comprising:

one or more processor cores;

a shared cache; and

a ring, wherein the ring connects the one or more processors and the shared cache;

2. The system of claim 1 wherein the one or more processor cores each include a private cache.

3. The system of claim 1 wherein shared cache includes one or more cache banks.

4. The system of claim 3 wherein the one or more cache banks is responsible for a subset of a physical address space of the system.

5. The system of claim 1 wherein the one or more processor cores are write-thru.

6. The system of claim 5 wherein the one or more processor cores writes data through to the shared cache.

7. The system of claim 1 wherein the one or more processor cores includes a merge buffer.

8. The system of claim 7 wherein data is stored in the merge buffer.

9. The system of claim 8 wherein the merger buffer purges data to the shared cache.

10. The system of claim 1 wherein the one or more processor cores accesses data from the shared cache.

11. The system of claim 8 wherein the merger buffer coalesces multiple stores to a same block.

12. The system of claim 1 wherein the ring is a synchronous, unbuffered bidirectional ring interconnect.

13. The system of claim 12 wherein a message has a fixed deterministic latency around the ring interconnect.